

IN THE CLAIMS:

Claims 1 through 36 and 40 through 54 were previously cancelled. Claims 37, 38, 55, 57, and 64 have been amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

37. (Currently amended) A method of preventing a circuit having a test test mode entry function from entering a subsequent test mode after the circuit enters a first test mode, comprising:
initiating a test mode blocking signal after the circuit completes the first test mode; and
exclusively controlling the test mode entry function of the circuit with the test mode blocking signal.

38. (Currently amended) The method in claim 37, further comprising generating the test mode blocking signal responsive to a final test latch of the circuit during the first test mode.

39. (Previously presented) The method in claim 38, further comprising originating the test mode blocking signal from the circuit.

40.-54. (Cancelled)

55. (Currently amended) The method of claim 37, further comprising resetting the test mode blocking signal in response to a reception of a reset prompt signal.

56. (Previously presented) The method of claim 37, wherein the initiating a test mode blocking signal is in response to receipt of a test-mode-end signal.

57. (Currently amended) The method of claim 37, wherein exclusively controlling with the test mode blocking signal includes gating the test mode entry function with one of an OR, NOR, AND, or NAND logic gate.

58. (Previously presented) The method of claim 37, further comprising preserving a state of an output of the circuit responsive to the test mode entry function in response to activation of the test mode blocking signal.

59. (Previously presented) The method of claim 37, wherein the test mode blocking signal is an output of the circuit responsive to the test mode entry function.

60. (Previously presented) The method of claim 37, wherein initiating a test mode blocking signal comprises:

initiating a latch mode; . . .
deriving an output signal from a logic operation performed on an input signal while in the latch mode; and
initiating the test mode blocking signal to disable the latch mode.

61. (Previously presented) The method of claim 60, wherein the deriving an output signal comprises deriving a plurality of output signals, and wherein the test mode blocking signal is one of the plurality of output signals.

62. (Previously presented) The method of claim 61, further comprising reestablishing the latch mode through a reset signal.

63. (Previously presented) The method of claim 62, further comprising reestablishing the latch mode exclusively through the reset signal.

64. (Currently amended) The method in claim 63, wherein reestablishing the latch mode through the reset signal comprises resetting the one of the plurality of output signals that initiated the input-leakout-test mode blocking signal.